ADAPTIVE CONFIGURABLE GATE ARRAY

This is a continuation of U.S. patent application Ser. No. 07/933,442, filed Oct. 5, 1992, now abandoned, which was a continuation in part of Ser. No. 07/803,944, filed Dec. 9, 1991 (abandoned) which was a continuation of Ser. No. 07/416,635, filed Oct. 3, 1989 (abandoned).

REFERENCE TO RELATED APPLICATIONS

This application describes subject matter common to and is copending with application Ser. No. 07/960,496, filed Oct. 13, 1992, by the inventors, and application Ser. No. 07/959,590, filed Oct. 13, 1992, by the inventors, which are divisions of their application Ser. No. 07/651,068, filed Feb. 4, 1991, by the inventors, now U.S. Pat. No. 5,217,916, which is a division of their application Ser. No. 07/416,635, filed Oct. 3, 1989, now abandoned.

FIELD OF THE INVENTION

This invention relates to a method of fabrication of integrated circuit chips or semiconductor wafers and, more specifically, to a "master slice" method of fabrication of those integrated types of circuits referred to as configurable gate arrays and application specific integrated circuits formed of configurable gate arrays. The invention also relates to a master slice configurable gate array integrated circuit wafer of novel structure that is adaptive to any size of application specific integrated circuit chip, a true "one size fits all" gate array, and to apparatus and processes therefor.

BACKGROUND

Integrated semiconductor circuits may be supplied to the electronic equipment manufacturer in the form of a small "chip" of rectangular shape, more specifically referred to as a "die", for bonding into a suitable package that is then mounted in a circuit board. The die is the end result of a fabrication process, "processing", which, as viewed from a macroscopic level, begins with a wafer of high purity semiconductor material, the "substrate", typically a grown single crystal silicon from which the wafer was sliced, with the wafer being of a size sufficient to support a number of copies of an integrated circuit to be processed simultaneously.

For example, an upper surface area defined by a wafer of four inches in diameter and a thickness of 50 mils represents one standard wafer size in present commercial practice. Many Integrated Circuits fit within that space. Through a series of processing steps, which are known, involving oxidizing, masking, which may be of the photolithographic stencil like technique or of the more modern laser or electron beam pattern formation apparatus, etching, metallizing, impurity doping and deposition a pattern of a large number of semiconductor devices are formed on the wafer's surface. Typically the semiconductors are arranged in discrete groups about the surface of the wafer with the groups spaced from one another by border strips, an effective "no man's land" between the groups. The semiconductors within the group are sometimes referred to as "cells". And each group of cells, referred to as an integrated circuit or simply IC, is of a generally rectangular shape and essentially forms an integrated circuit that provides a function specified by the circuit designer. This overall function may be a "calculator chip" that functions as the circuit for a calculator, a "computer chip" that functions as the element of a computer, or a "display chip" that serves as the electronic circuit to process signals for a visual display as example.

By such fabrication technique, many copies of a desired electronic circuit represented in the group of cells constituting an integrated circuit are reproduced simultaneously in a single processing of one wafer, providing obvious production advantage. As one of the final steps in the fabrication process the wafer is subsequently "diced" or, as otherwise stated, "sliced" using a saw, into frangible rectangular shaped sections and broken apart, effectively cutting the wafer into prescribed corresponding rectangular segments or dies, each of which contains an integrated circuit. Each IC chip from the wafer is a monolithic integrated circuit that is intended to perform the predetermined electronic functions specified by the circuit designer as in the examples earlier stated when the chip is installed in a circuit board or other electronic apparatus.

An individual integrated circuit, referred to in the preceding paragraphs as a collective group of cells, as viewed on a more microscopic level, contains very large numbers of semiconductor devices, referred to as transistors, interconnected by electrical wiring as achieves predefined electronic functions that collectively attain the overall function that the IC is intended to achieve. The IC is said to be formed of "cells", transistors of one form or another, arranged in an electronic circuit. The simplest form of cell may be referred to as a "gate". In turn the gate typically includes four transistors arranged in two pairs which are electrically isolated from the next cell. At a more elemental level, the gate may consist of only two transistors when the conventional "sea of gates" approach is used in which electrical isolation is achieved by having an associated pair of transistors wired to the electrically non-conducting or "off" state permanently.

Of those cells there are two major classes, used in what is usually called application specific integrated circuits, "ASIC", that are commonly used to allow circuit , designers to place large numbers of logic circuits on a single or common large scale or very large scale, collectively "LSI", integrated chip. One of these classes or types of cells is known as a standard cell, wherein each logical function is implemented as a custom designed circuit which can then be placed anywhere on the chip and be wired to other functions, circuits or cells. This provides a real convenience as the designer does not need to develop all the cells needed for the IC design. In this standard cell approach, the sizes of the devices or transistors and the layout of the circuits are optimized for each logical function so that density and performance characteristics are nearly comparable to a custom designed chip.

In the standard cell type of IC all steps in the fabrication of the wafer or chip are "personalized" for each particular design. Thus if any significant changes are to be made to the design, an entirely new mask must be made for every step in the fabrication process and the fabrication must again begin from a bare semiconductor wafer.

In contrast to the standard cell, gate array cells, typically referred to as "macros" are not personalized until the fabrication process reaches the first contact level to the conductive material which interconnects the devices or transistors in the gate array. That is, a typical gate array chip is formed by making rows of P-channel and N-channel transistors, if complementary metal oxide semiconductor, "CMOS", technology is used, arranged in functionally generic cells on the surface of the chip. For each discrete logic function available in the library of macros, a "person-